Proceedings of the RIC Project Day

Workgroups ‘Electronic Design’ and ‘Mechatronic Design’

Frank Kirchner (Editor)
Peter Kampmann, Marc Simnofske (Associate Editors)

07/2014
German Research Center for Artificial Intelligence  
Deutsches Forschungszentrum für Künstliche Intelligenz  
DFKI GmbH

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Prof. Wolfgang Wahlster  
Director
Proceedings of the RIC Project Day

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07/2014

Document D-14-05 des Deutschen Forschungszentrums für Künstliche Intelligenz (DFKI)
Abstract

This document is the current edition of an ongoing series of proceedings to document the workgroups’ topics, discussions and efforts at the Robotics Innovation Center of DFKI GmbH. The content of each of these editions represents presentations (talks and posters) of a project day which is organized by two workgroups, respectively.

Workgroups are formed by peers that are dedicated to a specific topic, so that they provide a platform for cross-project communication and knowledge transfer. In 2008 the workgroups started to present their results and past years work in an open presentation format called brown-bag talk, being a year after moved to more specialized so-called project days. Every year, since 2009, each workgroup presents results and past years work this project day. This format was extended to talk and poster presentations accompanied by the corresponding proceedings as a DFKI Document in 2014.

Zusammenfassung

Dieses Dokument enthält die aktuelle Ausgabe einer laufenden Tagungsband-Serie, welche die Themen, Diskussionen und Bemühungen der Arbeitsgruppen am Robotics Innovation Center der DFKI GmbH dokumentiert. Inhalt einer jeden Ausgabe sind die Vorträge und Poster eines Projekttags, der von jeweils zwei Arbeitsgruppen organisiert wird.

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1 Editorial

This is the second edition of a new format to document the efforts of the DFKI-RIC thematic workgroups. Workgroups are formed by peers and provide a means for cross-project communication on a deep content level and facilitate knowledge transfer amongst the peers. In 2008 we first started forming workgroups on specific topics around robotics and AI research. Among them were topics as 'system design & engineering', 'machine learning', 'planning & representation' as well as 'frameworks & architectures' and 'man-machine interaction'. These workgroups were established with the intention to provide a platform for interested DFKI-RIC personnel for discussing the start of the art, recent achievements, and future developments in the respective fields.

Over time the workgroups gathered a collection of material in form of presentations, short papers, and posters which were worthwhile to be presented also to the rest of the institute. Due to this development, in 2009, we started to have a project day once every quarter. Each project day provided a platform for two of the workgroups to present their material and to discuss it with the further colleagues of the institute. Nowadays, the project day is organized as a one-day workshop with oral presentations, poster sessions, and a free pizza lunch for everybody who attends. Until now, the talks and posters have only been collected on our servers but were not assembled in a citable document.

This format at present is the next evolutionary step and it aims at eliminating this deficit by compiling the material of the workgroups presented during a project day into a single, citable document of unified format. We will see which steps can be taken in the future to enhance the presentation quality of this material.

Frank Kirchner

This year’s third project day presented the material of the workgroups ‘Electronic Design’ and ‘Mechatronic Design’.

Within the workgroup ‘Electronic Design’ all kinds of electronic developments from sensors to microcontrollers and FPGAs to neuromorphic computing are discussed. Over the years this workgroup has established a powerful library of hardware ip-cores which are used in almost all of our robotic systems speeding up the initial integration significantly in the past time. Developers can build on a continuously growing set of verified building blocks having the possibility to concentrate on the implementation of controllers and behaviors of increasing complexity which is one of the main driving aspects in the future of robotics.

The constant monitoring of the current hardware developments allows the group to rely on state of the art techniques either on hardware itself or on the tools to debug and develop hardware projects. In the past time the constant attentive attitude toWhats new and will become future trends allowed the workgroup to handle to increasing complexity of large hardware projects.

This years presentations of the workgroup ‘Electronic Design’ are a perfect cross section of these topics. Initially, new trends on processing units like smartphone processors for robotics are reviewed followed by an impulse discussion about simplifying the calibration of the motor control by developing a configuration GUI. The talk is followed by a presentation of a nice little tool for debugging your design right at your desk by using a small logic analyzer. The idea of combining massively parallel programming approaches with a huge amount of serial processing units is addressed by a talk about current research dealing with dataflow processors. Three posters conclude the contribution of the workgroup ‘Electronic Design’ in this years project day. We are presenting a new high-speed communication allowing a impressive speed up of up to 300 MBit/second, attempts to standardize the development of our microcontroller section are presented and finally we have a very important poster presentation dealing with our working towards going to space.

The purpose of the workgroup mechatronic design is to discuss topics related to the development and assembly of innovative mechatronic systems which take advantage of modern materials and production technologies. Due to a high density of actuators and sensors, these systems are the basis for intelligent and autonomous robotic systems which offer a wide range of applications. At DFKI such systems have been developed for space, underwater, rehabilitation as well as for search and rescue. The focus of the contributions for the
project day 2014 was mobile robotic systems. These systems were used in several applications with different requirements. One ongoing challenge of developing systems for exploration tasks on earth or in space missions is lightweight construction to decrease power consumption. This was shown in the contributions about the EO smart connecting car 2 development, the SpaceBot rover and the Coyote II. In contrast to aforementioned, for wheeled systems in underwater applications other requirements come into play. Herein, systems with a density higher than water and waterproofed components are necessary. The current developments in this field were displayed in the presentation about the Moonwalk rover and the Sherpa II rover. Additionally, in the poster-session, we showed a device developed in the Nettun project used for changing cutting discs in a typical tunnel drilling machine. Up to now this dangerous work is done manually by a human.

We would like to thank the authors of the third project day 2014 for their contributions and for the effort to provide their material in a standardized format.

Peter Kampmann, Marc Simnofske
2 ‘Electronic Design’

2.1 ‘Current State in Electronic Design’ (ED-T-01)

Peter Kampmann

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Contact: peter.kampmann@dfki.de

Abstract

This presentation gives an overview about the current trends in electronic design that have been observed in the last year.

The developments are mainly driven by multicore solutions on a single chip, mainly driven by the smartphone industry. These cheap and power saving devices are worth having a look at for coming robotic systems. Simple programming or configuring of embedded devices is another major topic of the upcoming year.

The talk is finalized by giving a short overview over the coming talks in this electronic design project day.
Current State in Electronic Design

Project Day Electronic Design 24.07.2014

Strive for increase in autonomy

Datenvolumen aufgenommener Sensenwerte je Robotersystem

0 500 1000 1500 2000 2500
Datenmenge [MBa]

Jahr

2
“Big data” refers to datasets whose size is beyond the ability of typical database software tools to capture, store, manage, and analyze. This definition is intentionally subjective and incorporates a moving definition of how big a dataset needs to be in order to be considered big data—i.e., we don’t define big data in terms of being larger than a certain number of terabytes (thousands of gigabytes). We assume that, as technology advances over time, the size of datasets that qualify as big data will also increase. Also note that the definition can vary by sector, depending on what kinds of software tools are commonly available and what sizes of datasets are common in a particular industry. With those caveats, big data in many sectors today will range from a few dozen terabytes to multiple petabytes (thousands of terabytes).”

McKinsey Global Institute: Big data: The next frontier for innovation, competition, and productivity, 2011

Big Data

10 TBytes @ 30 Minutes

52 bytes @ 1 second

40 TBytes @ 1 second

1.7 Megabyte @ 1 second
Top 500 List of Supercomputers

- More than 3 million cores
- Intel Xeon @ 2.2 GHz
- 17 MW
- 6.4 MW for cooling
- 33.86 Petaflops

ARM based supercomputer

- Samsung Dual-Core-CPUs, Exynos 5, ARM Cortex-A15@1.7GHz
- Source: Mont Blanc
Clusters of embedded processors

• Tightly coupled processor arrays
  - Adapteva Epiphany
    ▶ Maximum configuration, E4KG4
    ▶ 4096 cores
    ▶ 5632 GFLOPS/s
    ▶ Power consumption: 70 GFLOPS/W
  - Tilera TILE TCPA
    ▶ Maximum configuration, TILE-Gx8072
    ▶ 72 cores @1.2 GHz
Clusters of embedded Processors

- **neuFlow**
  - Data-flow grid
  - Optimized for vision tasks
  - Contents of each processing tile
    - Streaming operators
      » MUL, DIV, ADD, SUB, MAX
    - Parallel 1/2D convolver
    - Configurable bank of FIFOs
      » Up to 10kB per PT
    - Configurable piece-wise linear or quadratic mapper
  - Virtex6 LX240T
  - LuaFlow: Dataflow language based on xFlow (http://code.google.com/p/xflow/)

Clusters of embedded Processors

- Application example, neoFlow

- Performance: 20 categories, 500x375 pixel @12 fps
Neuromorphic Computing

- Interest of mobile phone developers to transform smartphones into cognitive companions
  - Development of neuromorphic computing chips

Neuromorphic Computing

- Not (now) again the idea to fully mimic the human brain functions
  - process sensory data
  - learn from it
Neuromorphic Computing

- Neuron model
  - Computationally-efficient, Linear, two-Dimensional (COLD) neuron model
  - Model to support various flavours of spiking-neural networks

What is available today?

bStem – Development System
- Dual core Krait 405 @ 1.7GHz
- Adreno 320 GPU
- Xilinx Zynq FPGA

SOMANET
- An open source peripheral nervous system for machines
  - Communication Modules
  - Processor modules
  - Local Interface Modules
What is available today?

- Synapticon

Summary

- Standard CPU x86 architecture is more and more questioned
- Continuous growth of parallel data processing solutions
  - Using mobile processors with low power consumption
- “Cluster on a Chip” development building block for embedded supercomputing
- Neuromorphic computing is a new attempt to build brain like functions in optimized hardware
  - Powerful drivers (Human Brain Project, Qualcomm, lots of others universities in Europe and USA)
  - Timeframe for real use still unknown
- Hybrid solution: Learning algorithms on clustered embedded devices
Current topics addressed in our meetings

- Tooling, what makes your development work easier?
  - Talk by Hendrik Hanff

- The general idea of dataflow (-architectures, -machines)
  - Talk going into that direction by Moritz Schilling

- Signal Processing+Machine Learning on reconfigurable Hardware
  - Poster by Hendrik Wöhrle

- Space qualified electronics
  - Poster by Patrick Schöberl

- High speed communication for embedded devices HSComm
  - Poster by Florian Hühn

- Operating systems for small microcontrollers
  - Poster by Pierre Willenbrock

Thanks for your attention!
Abstract

"The Bus Pirate is a universal electronic open hardware tool to program and interface with communication buses and program various chips, such as AVRs from Atmel and PICs from Microchip Technology. A primary usage case for this device as intended by the designers is to "Eliminate a ton of early prototyping effort with new or unknown chips." Using a Bus Pirate, developers can use a serial terminal to interface with devices over a variety of hardware protocols, such as SPI and 1-Wire." [?] "Bus Pirate firmware v3.0 introduced a logic analyzer mode that works with SUMP-compatible open source logic analyzer clients. The logic analyzer can record 4096 samples at up to 1MHz, each channel has a selectable sample trigger. [...] The Bus Pirate will never be a substitute for a 'proper' logic analyzer, the hardware isn’t designed for it. The Bus Pirate can’t store a lot of samples, it can’t feed live samples very fast, and speeds are in the kHz range, not MHz. Despite the limitations of the Bus Pirate hardware, the logic analyzer worked well enough to examine decoded IR remote signals. It’s also well suited to debug environments where you can control the bus speed (and the Bus Pirate may already be connected for other reasons). It should also be able to look at most I2C traffic (400kHz clock)." [?] The presentation held on June the 19th 2014 gives a short introduction to the Bus Pirate in general. A more detailed description is given about the above mentioned logic analyzer mode."
2.2 ‘Bus Pirate’ – Hendrik Hanff

BusPirate
Hendrik Hanff

Projektag Sommer 2014

DFKI Bremen & Universität Bremen
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Direktor: Prof. Dr. Frank Kirchner
www.dfki.de/robotics
robotics@dfki.de
Introduction

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Introduction
- Bus pirate?
- Serial Bus Theory
- Means of debugging

BusPirate
- Features
- Logic Analyzer Mode
- User Interface

...hackable devices
Introduction

Normal mode

Using a Bus Pirate, developers can use a serial terminal to interface with devices over a variety of hardware protocols, such as I2C.

Bus analyzer mode
Introduction

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Serial Data bus
- I2C
- SPI
- 1-Wire
- UART
- HD44780 LCDs
- MIDI
- JTAG
- ...

...hackable devices
Introduction

Serial Data bus

- I2C
- SPI
- 1-Wire
- UART
- HD44780 LCDs
- MIDI
- JTAG
- ...

I2C

[Diagram showing I2C connections: uC Master, ADC Slave, DAC Slave, uC Slave]
**Introduction**

**Datasheet 2**

<table>
<thead>
<tr>
<th>P7</th>
<th>P6</th>
<th>P5</th>
<th>P4</th>
<th>P3</th>
<th>P2</th>
<th>P1</th>
<th>P0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Register Select</td>
</tr>
</tbody>
</table>

- **P2** - **P0** REGISTER (Note 13)
  - 000 - Temperature
  - 010 - Configuration
  - 011 - \( T_{\text{HIGH}} \)
  - 001 - \( T_{\text{LOW}} \)
  - 100 - Control / Status
  - 111 - Identification

...hackable devices
Introduction

Datasheet 3

\[\text{...hackable devices}\]

I2C sample session

\[\text{...hackable devices}\]
Introduction

Conversational problems

I2C: Possible problems

- Wrong I2C slave address
- Wrong I2C slave sub-address
- Slave is busy
- Wrong communication speed
- I2C slave broken
- Wrong voltage level
- ...
Introduction

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Serial Bus Theory
Means of debugging

BusPirate
Features
Logic Analyzer Mode
User Interface

Stare on code/gdb/simulation

```
when ads1015_send_slave_addr_write =>
  i2c_ctrl_s <= decode_i2c_ctrl(write);
  mstr_din_s <= ads1015_slv_adr_i & WRITE_C;
  if rec_ack_s = '1' then
    timeout_cnt_en_s <= '0';
    i2c_ctrl_s <= decode_i2c_ctrl(write);
    ads1015_fsm <= ads1015_set_config_reg_addr;
  else
    ads1015_fsm <= ads1015 fsm;
  end if;
```
Introduction

Oscilloscope sample session

Passive bus analyzer
Introduction

Passive bus analyzer sample session

2.2 ‘Bus Pirate’ – Hendrik Hanff

...hackable devices

Hmmm...
BusPirate

Contents

Introduction
- Bus pirate?
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- Means of debugging

BusPirate
- Features
  - Logic Analyzer Mode
  - User Interface

Open Design
- Free (CC, GPL, 30$)
- PIC24FJ64GA002, voltages, IO, ADC...

Flexible Firmware
- LogicAnalyzer, I2C, and whatnot
- Interpreter, Bootloader, macros, online help

no here, take my money! tool – more like look, it can make coffee!
BusPirate

Open Design
- Free (CC, GPL, 30$)
- PIC24FJ64GA002, voltages, IO, ADC...

Flexible Firmware
- LogicAnalyzer, I2C, and whatnot
- Interpreter, Bootloader, macros, online help

no here, take my money! tool – more like look, it can make coffee!

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BusPirate

Bus Pirate vs. Yokogawa SB5710

<table>
<thead>
<tr>
<th></th>
<th>Bus Pirate</th>
<th>Yokogawa Serial Bus Analyzer</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSamples/s</td>
<td>1</td>
<td>250 (limited by probe)</td>
</tr>
<tr>
<td>Sample memory</td>
<td>4k</td>
<td>6,25M</td>
</tr>
<tr>
<td>Nr. of input pins</td>
<td>5</td>
<td>32</td>
</tr>
<tr>
<td>Costs</td>
<td>€30</td>
<td>€14000</td>
</tr>
</tbody>
</table>

---

**Sampling Frequency**

**BusPirate**

**Yokogawa**

1 MS/s 250 MS/s
2.2 ‘Bus Pirate’ – Hendrik Hanff

BusPirate

Sample Memory

**BusPirate Yokogawa**

![Diagram of 4kWords 6,25MWords]

Logic channels

**BusPirate Yokogawa**

![Diagram of 5 Pins 32 Pins]

Universität Bremen

...hackable devices
BusPirate

Costs

BusPirate \( \rightarrow \) Yokogawa

30EUR \( \rightarrow \) 35.000EUR

OLS - Open Logic Sniffer (1)
BusPirate

OLS - Open Logic Sniffer (2)

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BusPirate
Plug and Play

guybrush@home:~$ cu -l /dev/ttyUSB0 -s 115200
Connected.
$ RE
Bus Pirate v3.5
Firmware v6.1 r1676  Bootloader v4.4
DEVID:0x0447 REVID:0x3043 (24FJ64GA002 B5)
http://dangerousprototypes.com
HI2>

...hackable devices
BusPirate

Help?

<table>
<thead>
<tr>
<th>General</th>
<th>Protocol interaction</th>
</tr>
</thead>
<tbody>
<tr>
<td>?</td>
<td>This help (0) List current macros</td>
</tr>
<tr>
<td>=X/IX</td>
<td>Converts X/reverse X (x) Macro x</td>
</tr>
<tr>
<td>~</td>
<td>Selftest [ Start Stop</td>
</tr>
<tr>
<td>#</td>
<td>Reset the BP</td>
</tr>
</tbody>
</table>
| $       | Jump to bootloader (Start with read)
| @/X     | Delay i us/us (Stop)
| a/A/A   | AUXPIN (low/Hi/READ) "abc" Send string |
| b       | Set baudrate 123 |
| c/D     | AUX assignment (aux/CS). 0x123 |
| d/D     | Measure ADC (once/CONT.) Send value |
| f       | Measure frequency |
| g/h     | Generate PWM/Servo CLK hi |
| i       | Commandhistory |
| L/L     | Bitorder (mb/LSB) DAT hi |
| m       | Change mode DAT lo |
| o       | Set output type DAT read |
| p/P     | Pullup resistors (off/ON) Bit read |
| s       | Script engine Repeat e.g. r:10 |
| v       | Show volts/states Bits to read/write e.g. 0x55:2 |
| w/W     | PSU (off/ON) Usermacro x/assign x/list all |

BusPirate

I2C!

<table>
<thead>
<tr>
<th>I2C &gt;?</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. HiZ</td>
</tr>
<tr>
<td>2. I-WIRE</td>
</tr>
<tr>
<td>3. UART</td>
</tr>
<tr>
<td>4. I2C</td>
</tr>
<tr>
<td>5. SPI</td>
</tr>
<tr>
<td>6. 2WIRE</td>
</tr>
<tr>
<td>7. 3WIRE</td>
</tr>
<tr>
<td>8. LCD</td>
</tr>
<tr>
<td>x. exit(without change)</td>
</tr>
</tbody>
</table>

(1) >4
- Set speed: 1. 5KHz 2. 50KHz 3. 100KHz 4. 400KHz

(1) >3
- Ready I2C>
BusPirate

Who's there?

I2C>(0)
0.Macro menu
1.7bit address search
2.I2C sniffer
I2C>XP
POWER SUPPLIES ON
Pull-up resistors ON
I2C>(1)
Searching I2C address space. Found devices at:
0x00(0x00 W) 0x90(0x48 W) 0x91(0x48 R)
I2C> [0x90 0x42]
...

Finished

Questions?
Abstract

This talk covers the potential benefits of the general idea of reactive system programming to robotics. Starting with a definition and taxonomy of reactive systems, some famous examples - namely dataflow architectures are presented and grouped into the greater picture. Given this introduction, a first realization of a hybrid dataflow architecture on reconfigurable hardware is explained. Based on this architecture, the benefits as well as future steps towards reactive robotic systems are discussed.
Distributed Reactive Systems
Moritz Schilling

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  Taxonomy

Dataflow Architecture Subclass
  Static Dataflow Machine
  Dynamic Dataflow Machine

Hybrid Dataflow Architecture
  Data-Driven Processor Network
  Results

Future Work
  Motivation
  Potential Benefits
  First Ideas
Introduction

What are Reactive Systems?

- Program represented as a data dependency graph
- Basic building blocks: behaviours/nodes and arcs
- Continuous interaction with some environment
- Evaluation triggered by (need for) input
Introduction

Taxonomy of Reactive Systems

- Evaluation
- Directionality
- Concurrency
- Determinism
- Timing and Safety

Dataflow Architecture Subclass

- Dataflow Architecture
- Evaluation
- Directionality
- Concurrency but Parallelism
- Determinism
- Timing and Safety

Dataflow Architecture Subclass

- Data-Driven
- Demand-Driven
- Unidirectional (←)
- Multidirectional (→)
- Depends on Transport Layer

Dataflow Architecture Subclass

- Data-Driven
- Demand-Driven
- Unidirectional (←)
- Multidirectional (→)

Evaluation

Directionality

Concurrency

Determinism

Timing and Safety
Dataflow Architecture Subclass

Static Dataflow Machine

- A node is evaluated if
  - all operands are available
  - no data item on output arc
- Only one data item is allowed on any arc
- Synchronisation through acknowledgements

Dynamic Dataflow Machine

- A node is evaluated if
  - all operands of the same context are available
- Any number of data items on any arc allowed
- Synchronisation depends on arc definition (e.g. bounded buffer)
Hybrid Dataflow Architecture

Data-Driven PicoBlaze Processor

- Based on Xilinx KCPSM6 PicoBlaze
- Up to 256 input ports
- Up to 8 output ports
- 8 Bit data bus
- CPU sleeps if
  - operands are not available
  - previous results have not been sent yet
  - user requests it

Working Examples

- Pipeline
  - Up to 200 PicoBlaze cores
  - 1 input, 1 output
- Parallelism
  - Example:
    \[ Y = X^2 + 2X \]
- Recursion
  - Initial values can be assigned
  - Important for dynamic systems
Hybrid Dataflow Architecture

Evaluation

Advantages
▶ Very small footprint
   1 BRAM16/core
   ≃ 200 LUTs/core
▶ Working proof-of-concept
▶ Reduced power consumption when idle

Disadvantages
▶ Static connections
▶ No instruction level parallelism
▶ Limited instruction set (no MULT)
▶ Only 8 Bit data width
▶ No C compiler

Future Work

Distributed, Reactive System Model

▶ Multidirectional graph of processing nodes
  ⇒ Robotic system = Distributed system
▶ Sensor-Actor loop
  ⇒ Data-driven system

Partial Graph of processing nodes in Charlie
Future Work

Potential Benefits

- Utilization of limited processing resources
- Unified task interfaces and data distribution
- Reduction of unnecessary computation and power consumption
- Exploitation of pipelining effects and parallelism
- Hierarchical, distributed control loops
- Incremental development

First Ideas

- Asynchronous channels with SWSR fifo semantic
- Data-driven task execution
- Automatic mapping of tasks to heterogenous hardware
- Interface implementations for different hardware components (FPGA, uC, ...)
- Reassignment of tasks depending on demands
- Acceleration of development by visual programming
Future Work

Example of SW to HW Mapping

Thank you for your attention!
2.4 ‘HsSerComm: A Fast, FPGA based, low power communication interface’
(ED-P-01)

Florian Hühn(1)

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Abstract

An implementation of a serial communication line for data communication between joints of a robotic system is presented. The new design pushed the achievable datarate from a former 500kBaud/s to 500MBaud/s without the need for new cables or connectors. Furthermore, it lowered the bit error rate to less than $10^{-10}$ in a typical use case scenario.

The implementation is characterized by using very little board space – even less than the previous, 500kBaud/s solution – and being easy to implement in an FPGA while consuming only very little FPGA resources. It makes use of the dedicated IO hardware that is available in the FPGA.

On the data link layer it adds 10 control words which can be used for various cases, superseding previously used escape sequence generators.
Keeping track on the demand for ever higher communication rates

The availability of more and more high resolution sensors onboard a robotic system in combination with software that gets more dynamic and decentralized has led to an increasing need for higher bandwidth communication lines inside these robotic systems.

In a tightly packed robot, space is a very limited resource — in terms of physical volume as well as in available resources inside the FPGAs. Striving for the smallest footprint possible, common standards like Ethernet were all ruled out, giving reason to develop a specialized solution that fulfills all requirements.

Whereas the previously used solutions where limited to 1MBaud, the implementation that will be discussed here can provide up to 500MBaud over the same wire. Moreover it adds 10 control words to the list of transferrable symbols, eliminating the need for escaping sequence generators and provides an electrically robust interface with 1kV galvanic isolation.

Hardware interface

The hardware interface only utilizes one pair of twisted copper lines per direction to transmit its full 500MSym/s. The cable that is to be used in our robots is not specified for its RF characteristics but measures to have a wave impedance of around 100 Ohms with a pretty high attenuation factor towards higher frequencies which further helps to reduce reflections which might be caused by an improper termination.

To keep the mechanical footprint low, LVDS is used for the physical layer, for which every modern FPGA contains dedicated line driver and receiver modules. To protect the sensitive FPGA ports and provide a galvanic isolation barrier a low profile pulse transformer is used.

Figure 1 depicts the whole electrical interface structure:

- Nothing more than the FPGA, a pulse transformer and a decoupling capacitor for the cable shielding is required, keeping physical space requirements to an absolute minimum. On the receiving side the internal termination resistor of the FPGA is activated.

Fig. 2: Block diagram of the FPGA implementation

FPGA implementation

The FPGA implementation makes heavy use of the dedicated hardware blocks ("IOB") which are built into the FPGA right between the slices and the actual I/O pins.

On the transmitting side an incoming word is encoded via 8b10b into a 10 bit long transmit word, serialized by a factor of 5 into chunks of 2 bit each and then further serialized by an OSERDES2 hardware block which directly feeds the LVDS driver.

On the receiving side, the LVDS receiver passes the received signal, which is still time continuous, through a delay line which output two copies of the same signal with ¼ of a symbol length delay between them. They are sampled simultaneously by two ISEDES2 blocks which also deserialize the stream by a factor of 4. This results in 8 sample points over the length of two symbols in every clock cycle, which are then further processed in normal slices which run at 250MHz. After passing the synchronization and tracking stages, the detected 10 bit words are isolated and decoded by the 8b10b decoder.

The actual implementation on a Spartan6 uses 38 slices plus one BRAM for the receiver and only 13 slices plus one BRAM for the transmitter.
2.5 ‘TRL 5 for Space BLDC Electronics’ (ED-P-02)

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Abstract

The Poster describes the development of a so called technology readiness level 5 BLDC electronic for space application - which means that it will be validated in space relevant environment. It describes initially some problems in space as for example vacuum, radiation or critical temperature. This section is followed by an abstract on how to handle those malfunctions by selecting the right electronic components; add safety by redundancies to all safety relevant circuit parts and how to protect critical components. The last section describes how to resist radiation by selecting the right components as for example enhancement-mode Gallium-Nitride-on-Silicon field-effect transistors (eGaN-FETs) for the motor driver power stage.
2.5 ‘TRL 5 for Space BLDC Electronics’ – Patrick Schöberl

TRL 5 for Space BLDC Electronics
How to reach Technology Readiness Level 5 requirements

Patrick Schöberl, 2014

The story of “some” problems in Space

- “Far away problem” - you cannot fix problems after launch
- Temperature - mostly too cold or too warm
  - e.g. on Moon: -160°C at night and +130°C at day
- Vacuum - out gassing of components and no heat dissipation
  - No possibility to cool down by a fan
- Radiation - a reliable way to destroy semiconductors

Ways to solve “some” problems in hardware

- “Far away problem”
  - Robustness, reliability, fault protection and redundancy
  - Temperature - use components with higher temperature range, depends on the mission and system setup
    - e.g. op. temp at minimum in range of -40°C to +85°C
- Vacuum
  - Use of special glue and finish
  - Use mechanical structure to dissipate heat
  - Try to produce as less heat as possible – each mW counts

How to resist the malefactor radiation by hardware

- Use of a metal case as simple protective shield
- Triple modular redundancy ADC module with 8x 12Bit channels
- Dual communication interface
- Multiple “over current detection” switches
- Flash based FPGA for improved SEU resistance
- Derating of components to prevent failures
- eGaN-FET (Gen2) for improved resistance against SEB/SEGR
  - Can be used up to at least 1MRad without performance degradation
  - Higher level of SEE tolerance compared with silicon power MOSFETs special designed for GML/GMV
  - Low gate charge and low “On” resistance
- Fault back solution for sensors
- Use tested COTS parts (for example tested by particle accelerator)
- Keep it simple

Redundancy

Multiple redundancies are used to harden the design, e.g. the ADC module. Three different 8 channel ADCs are used by the different vendors. Each ADC is additionally protected by an “over current detection switch” to prevent latch ups. The FPGA acts as voter.

The interface is implemented two times as well. In the same style as the ADC module each implementation uses different vendors and devices for the same functionality.

Over heating and over voltage are limiting factors to electronics, therefore it is possible to measure some known hotspots and levels by using the ADCs. But a second fault back solution will detect over voltage or over temperature without using ADCs.

It is possible to use hall sensors and/or BEMF to commutate the BLDC Motor – in case of a defect, a second commutation style is usable.

Supported by:

Universität Bremen
2.6 ‘Signal Processing and Machine Learning on Reconfigurable Hardware using reSPACE’ (ED-P-03)

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Abstract

In this poster, the framework reSPACE for signal processing and machine learning on reconfigurable hardware is introduced. It allows to rapidly develop application-specific, FPGA-based hardware accelerators to speed up certain computational intensive data processing tasks. The underlying computational model is the static heterogeneous synchronous dataflow computing paradigm.

In order to make the hardware accelerators accessible, it utilizes various model-based software generation techniques to automatically generate device drivers and test facilities for simulation- and hardware-based verification.
Signal Processing and Machine Learning on Reconfigurable Hardware using reSPACE

A Framework for the Development of Mobile or Embedded Signal Processing Devices

Welcome to the Jungle

In the twilight of Moore’s Law, the transition to multicore processors, GPU computing, and field-programmable gate arrays (FPGA) computing, and fault-tolerant processing, etc., a single-mindedness computing approach is associated with the production of large-scale systems. The idea of flexible, dataflow-oriented systems, where a single computer-intensive application will be used to harness different kinds of cores, is becoming increasingly important in this new data era. The new task is not more powerful hardware but how flexible it is to use. The key to the hardware jungle is the Dataflow Graph (Flynn [3]).

Properties of Machine Learning and Signal Processing Algorithms

Computational Operations in Machine Learning and Signal Processing

Deep learning is a buzzword for neural nets, and neural nets are just a stack of canonical operations. The actual problems with conventional processors is that these canonical operations are not specialized for typical signal processing operations.

Dataflow Paradigm

Heterogeneous Dataflow Computing

The dataflow hardware in the reSPACE framework is a Data Flow Machine that exactly matches the Dataflow Graph (Flynn [3]).

Figure 1: Small digital circuit elements, so-called logic slices, can be connected as required to form specific circuits that implement a specific functionality. These are connected by a flexible interconnect. Ideally, FPGAs contain special elements for signal processing (DSP slices) and data buffering (Block RAMs).

FPGAs can be pro-grammable for specific tasks, which is a great advantage of these hardware accelerators. It allows the development of very specific hardware accelerators.

Figure 2: Dataflow paradigm and verification for MLPs. By using Testbenches, the reSPACE framework is extended to support the development of mixed-signal systems, which are popular for machine learning such as MLPs [2] and used for embedded signal processing [5].

The framework reSPACE is based on the static heterogeneous synchronous dataflow computing model, which has been proposed by Flynn as the Dataflow Graph in the 1970s. reSPACE allows the development of mixed-signal systems, which are popular for machine learning such as MLPs [2] and used for embedded signal processing [5].

Conclusions and Future Work

We discussed the necessity, requirements and state of the framework reSPACE that supports the implementation of dataflow accelerators for machine learning and signal processing. This will help in the future to speed up the way towards reconfigurable hardware. We conclude the framework reSPACE is ready for the implementation of a full-fledged dataflow processor.

References

Abstract

The Poster Operation Systems for small Microcontrollers describes when an operating system may be needed on a small micro controller and then compares the memory usage, availability of standard APIs, driver and platform support and licenses of seven small operating systems.
More functionality on small microcontrollers

In a world of ever more powerful microcontrollers, ever more functionality gets put into microcontrollers. Unfortunately, this increases the complexity of scheduling the execution of all these functions and communication between them. Additionally, most of the time, these functions, if not completely unrelated to underlying hardware, are specifically implemented with a certain microcontroller family.

Operating systems generally solve these problems by allowing to divide functionality in processes that are scheduled and executed in turn by the operating system(without or with very little help by the processes), providing interprocess communication mechanisms and abstracting away hardware details using device drivers.

Operating systems can provide additional features, especially process separation to privilege and protect processes from others, but this generally requires special hardware(Memory Management Unit) that is not available on small microcontrollers.

Drivers and hardware abstraction layer

All tested operating systems provided a hardware abstraction layer, that is, a generic interface to interface with certain hardware classes. All operating systems had support for serial ports and general purpose input/output pins. The most comprehensive HAL can be found in ChibiOs, Ecos, RTEMS.

Use of standard APIs

Most of the tested operating systems did not use standard POSIX or similar APIs. ChibiOs and RIOT OS can use newlib, which provides some standard Unix functions, depending on the amount of syscalls implemented by the user application. RTEMS and Ecos use their own C library, so these can use the complete set. Additionally, Ecos and RTEMS support the POSIX threading API.
3 ‘Mechatronic Design’

3.1 ‘Enhancing Mobility Using Innovative Technologies and Highly Flexible Autonomous Vehicles’ (MD-T-01)

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Abstract

Automobiles of today combined with human driving behavior as well as very different levels of driving experience results in massively congested inner city traffic on a regular basis. Smaller cars with intelligent assistance features and autonomous driving capabilities can help release the tension of traffic. EO smart connecting car 2 is a concept car to fulfill these new requirements. It features many normal driving, turning on the spot, driving sideways and many autonomous functions as laid out within the presentation.
3.1 ‘Enhancing Mobility Using Innovative Technologies and Highly Flexible Autonomous Vehicles’ – Timo Birnschein

Enhancing Mobility Using Innovative Technologies and Highly Flexible Autonomous Vehicles

Or: Why cars should go sideways

Dipl.-Inform. Timo Birnschein
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How we see cars at present …

Foto: Opel
Foto: Toyota
Foto: Volkswagen

Dipl.-Inform. Timo Birnschein
Current Problems in Cities

Dipl.-Inform. Timo Birnschein

Imperial College Urban Energy Systems Project, http://www3.imperial.ac.uk/energyfutureslab/research/grandchallenges/urbanenergysystems

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World Population Estimates

- 50% of Global Population – Currently live in dense urban areas

The urban and rural population of the world, 1950-2050

- Urban population
- Rural population

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Dipl.-Inform. Timo Birnschein
Current Problems in Cities

90% of population growth will be in urban areas:
80% of the wealth

60% urban energy use:
Transportation + building operations

40% total gasoline use:
cars looking for parking (in congested urban areas)

new concept of SMART City & Car is needed

Current Problems in Cars

- Private cars: Major source of pollution and carbon emissions; massive congestion, parking, and noise problems
- Public Transportation: Does not cover the entire city; inconvenient and inflexible schedules
- First Mile-Last Mile Problem of public transit: not solved
- The vehicle concept didn’t change for over 125 years
1892 William Morrison

First successful electric car by William Morrison 1892
4hp, front-wheel-drive, steel-clad wooden tires, max. 32km/h, 24 battery cells under seats. recharging every 80km

Dipl.-Inform. Timo Birnschein

1900 Lohner-Porsche

Lohner-Porsche using wheel-hub motors (115kg each) and a 300Ah battery – which weights 410kg – gasoline motor as range extender
2x7hp max, front-wheel-drive, max. 50km/h, 44 battery cells under seats. recharging every 50km

Dipl.-Inform. Timo Birnschein
Change Major Design Constraints

- Remove central engine (combustion, hybrid, electric)
- Remove exhaust
- Remove Tanks – gasoline / diesel and hydrogen
- Remove heavy and lengthy drive train parts and gears
- Reduce overall size and weight
- Reduce energy consumption, complexity
- Make use of new technology, e.g. electric wheel hub motors
- Construct lightweight chassis and body
- Add new and useful features and drive modes for cities
- Remove charging cable add docking interface
- Make driving as easy and accessible as possible

EO smart connecting car

- Idea of a folding car for roadtrains born in early 2010
- A team of scientists started working on the first highly innovative robotic car in August 2010

- Publication on CeBit and HMI 2012
- Overwhelming public response despite the looks...

- Only a feasibility demonstrator for a new category of mobility…
**EO smart connecting car**

- **Modular**
- **Changeable Morphology**
- **Autonomous Driving**

Subproject “Innovative Technologies Electromobility (ITEM)” – main project “Model Region Electric Mobility (PMC)” – Module 2 “Intelligent Integration of Electric Mobility”

Funded by the German Federal Ministry of Transport, Building and Urban Development (Grant Nr. 03ME0400G)

Program coordination is carried out by the National Organization Hydrogen and Fuel Cell Technology (NOW GmbH).

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**Development of EO smart connecting car 2**

- Starting in October 2011, ten scientists began parallel development of requirements as well as hard- and software

Water cut suspension module for first experiments with 90 degree steering
Development of EO smart connecting car 2

- Starting in October 2011, ten scientists began parallel development of requirements as well as hard- and software.

Functional test platform ready in July 2013

Chassis manufacturing finished in October 2013
Starting in October 2011, ten scientists began parallel development of requirements as well as hard- and software.
Docking Interface construction finished in November 2013

Docking Interface integration finished June 2014

New motor housing with integrated brakes
CAD design in February 2012
Development of EO smart connecting car 2

Active Battery Management System with high current balancer

High Energy Ultra Cap Charger for storing recuperative energy

University of Bremen

Vehicle Control Unit, Peripheral Control Unit, Power Supply and SSR

Axial internal Analog Sensor Array
Features of EO smart connecting car 2

- Physics simulation based optimization of all working loads
- Innovative and useful drive-modes and features:
  - Drive normal
  - Drive sideways
  - Turn on the spot
  - Drive diagonal (only accessible when driving autonomously)
  - Fold the car to shrink it’s size
  - Foldable docking interface for charging stations / extension modules
  - Sportive and modern body design
- Weight: 750kg
- Max Speed: 65kp/h – 70 kp/h
- Batteries: 50V, 100Ah, 5KWh, can be extended to 10KWh
Autonomy for parking, docking and driving

- Integration of sensors currently in progress
- SpaceBot mapping, navigation, and guidance software stack will be ported and adjusted to work with EOscce2

Velodyne Lidar HDL-32E – Image taken at DLR SpaceBot Cup by Artemis Rover

Blutechnix Sentis ToF - M100

Prosilica GE1900

Conclusion

- A more radical change in car design for mega cities is necessary
- Fully autonomous functions can rise quality of life
- Wheel hub motors offer an unknown freedom over design – completely new designs and much more flexibility are possible
- Virtual road trains can release tension in dense traffic

Technology is ready, we just need to use it
Outlook

• Autonomous parking on known and unknown parking areas
• Service functions for car sharing:
  ▪ One person collects several cars and distributes them to all necessary pick-up locations
  ▪ Charging several cars at one docking station and being able to pick the one with the proper SoC for the specific journey
• Experiments, Testdrives, Evaluation, and Optimization

• Fully autonomous driving from point A to point B
3.2 ‘Sherpa II - TransTerra’ (MD-T-02)

Florian Cordes(1)

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Abstract

The presentation focuses on the hybrid walking-driving rover Sherpa and its successor SherpaTT. Sherpa(TT) has an active suspension system to actively conform to irregular terrain. The mechanical design of the first version is discussed, its benefits and drawbacks are highlighted. The derived design improvements are presented. The talk concludes with the first steps in setting up a new motion control system for SherpaTT, that were conducted in DFKI’s MARS simulation environment.
Why Active Suspension?

- Passive, most prominently Rocker-Bogie
  - Mechanics do the adaption, no control needed
  - Ground wheels have to give thrust needed to drive other wheels over obstacles
- Active: Control needed to be active
  - Thus: Higher computational efforts for (“low-level”) locomotion
- Active suspension provides higher locomotion capabilities in the long run
  - Free the system from stuck situations
  - Maneuverability: Obstacle size, non-continuous path of wheels possible
  - Reconfiguration space from driving to walking
  - Combines benefits from rolling and walking behaviors
Sherpa - Overview

- Variable footprint
  - Track width: 660mm to 2610mm
  - Length: 2610mm to 660mm
  - Body height: -189mm to 711mm
- Mass: 160kg
- Max speed: ca. 500mm/s (HD 1:80)
- Torque per wheel: 59 Nm
- No. of active DoF: 6 per leg + 6 arm = 30 DoF
- Manipulator is strong enough to support the rover with two legs lifted
- Equipped with general purpose electro mechanical interfaces (EMI)
  - 4 passive/male around manipulator
  - 2 active/female (1x manipulator, 1x bottom of central body)

Role of Sherpa in MRS

- Current design developed as part of a multi-robot system
  - Transport walking scout robot
  - Transport and assemble modular payload-items
  - Cover large distances in "semi-rough" terrain, walking scout robot is used for advancing into crater environment
### Drawbacks Identified

- Two joints Pan+Lift for placing the wheel in $(x,y,z)$
  - Underactuated/ Interdependency of DoF
- Tilt and Flip rarely used: Flexible wheels sufficient for small scale ground adaption
- High stow volume (compact pose not possible)
  - Approx. $2.25m \times 0.8m \times 1.35m = 2.43m^3$
- Active Partner for docking to bottom interface needed
  - New scenario requires pick-up of passive payloads with bottom interface
- Missing F/T-sensor for sophisticated ground adaption
- Multiple different actuators increase maintenance efforts

### Design Studies for Design Upgrade

- Goal is a reduced, compact stow envelope
- More flexibility in body pose desired
- Asymmetric body is not optimal for manipulator usage
  - Neither for use in manipulation nor in case of locomotion support
Design Improvements

- **Conceptual**
  - Keep four identical Legs, symmetrical arranged around central body
  - Elastic wheels for small scale ground adaptations
  - Central manipulator for payload positioning and locomotion support
  - Base camp storage underneath body

- **Project / mission requirements**
  - Passive base camp needs to be picked up
  - Modular expansion using modular payloads and a common electro-mechanical interface (EMI)

- **Features**
  - Compact storage pose
  - Increased range of movement/work space of legs
Suspension Re-Design

• Five Degrees of Freedom
  ▪ Three positioning the wheel
  ▪ Two for wheel orientation and wheel drive

• Advantages
  ▪ Increased range of movement for Wheel Contact Point
  ▪ Zero Scrub Radius
  ▪ Linear Actuator in “pull” configuration (higher precision due to lower mechanical slackness)

• Types of actuators
  ▪ Two linear actuators (push rods)
    ▪ Used in serially coupled parallel structures
  ▪ Three rotational actuators

Joint Max Positions (Zero Positions)
Joint Max Positions (Outer Up)

Joint Max Positions (Outer Down)
Joint Max Positions (Zero Positions)

Joint Max Positions (Inner Up)
Joint Max Positions (Inner Down)

Modular Actuator Concept

<table>
<thead>
<tr>
<th>Electronic</th>
<th>Motor</th>
<th>Gearbox</th>
<th>Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>„BLDC-Stack“</td>
<td>Motor-Module ILM50</td>
<td>Gearbox CPL17</td>
<td>Linear-Actuator Kit</td>
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<tr>
<td>- Power Electronics</td>
<td>- 0.50 Nm</td>
<td>- 1:30, 1:50, 1:80, 1:100, 1:120</td>
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<tr>
<td>- Local Control</td>
<td>- 3500 rpm</td>
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<td>- Speed</td>
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<td>- Communication</td>
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<td>Motor-Module ILM70</td>
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<td>- 0.74 Nm</td>
<td>- 1:30, 1:50, 1:80, 1:100, 1:160</td>
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<td>- 3500 rpm</td>
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<td>HighTorque Gearbox</td>
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<td>- 1:3000</td>
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</table>
Implemented Actuator Types

- Three types implemented
  - A nominal 29rpm / 55Nm
  - B nominal 35rpm / 74Nm
  - C nominal 1.1rpm / 433Nm
- For Lift and Knee Type A + Linear Kit

Wheel Drive and FTS

- Flexible wheel design
- Adapts to small ground irregularities
- For now: planned material is rubber
- 3 to 4 water jet cut discs allow testing different profiles and different wheel widths
Sherpa Control – First Steps

- First version of Sherpa had own locomotion controller, HL-behaviors in Rock
- New locomotion controller integrated in Rock
  - Simulation based development
  - Modeled kinematics
  - Planar (omnidirectional) drive behavior
  - No ground adaptations so far
- Planned
  - Active ground adaption using FTS and IMU
  - Alternative drive modes

Outlook / Next Steps

- Electro-mechanical integration of new suspension legs (1x Testleg)
  - Currently work-in-progress
  - Joint electronics are ready
- Low-level control
  - Joint control
  - Joint communication
  - Leg control
- Locomotion control using simulation
  - Implement adaption behaviors
  - Implement alternative locomotion modes
  - Port to physical system after electro-mechanical integration
Thank you!
3.3 ‘Coyote II Development’ (MD-T-03)

Roland Sonsalla(1)

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Abstract

The talk introduces the design and evaluation of the micro scout rover Coyote II. First, the general operational approach of the scout rover within the FASTER mission set-up is introduced and second, a technical overview of the system itself is given along with a subset of different locomotion and mobility tests.
Project Outline

**FASTER**  
Forward Acquisition of Soil and Terrain data for Exploration Rover

Funded by the 7th Framework Programm of the European Commission (GA 284419)
Scout Rover Operation Approach

- Scout rover acting as semi-autonomous remote sensor of a primary rover
- Normal scout rover traversal sequence:
  - Both rovers close to each other
  - Receive position and waypoints for ~4 m traversal
  - Odometry based trajectory following
  - Soil sensing for hazard detection during traversal
  - In case of hazard: path replanning by primary rover

Key Design Driver

- Scout rover mass: < 20 kg (incl. payload)
- High all terrain mobility providing:
  - Traversability of slopes up to 25°
  - Static stability angles of 40 degrees in all directions
  - Min. average speed of 1.25 cm/s
- Design challenges
  - Rover steering (wheel design)
  - Wheel sinkage on soft soil vs.
  - High mobility on rough terrain vs.
  - Digging over of soft soil
Coyote II: Technical Overview

- Boundary box: 850 x 580 x 410 mm
- System mass: 9.2 kg (without payload)
- Wheel torque: 28 Nm
- Average power: 75 W

Locomotion and Steering Concept

- Locomotion Concept to meet design challenge:
  - Front: Hybrid legged-wheels
  - Rear: Spherical helical wheels

- Point turn: side-to-side steering
  - Introduce sideward motion by helical wheels
  - Shift point of rotation to front axis
  - Reduction of soil disturbance

- Continuous steering
  - Apply different wheel speeds to left and right rover side
Side-to-Side vs. Skid Steering

Common Skid Steering

Side-to-Side Steering

Wheel Evaluation

Point Turn Test Bench Overall Power Consumption

- Asguard Wheels #1
- Asguard Wheels #2
- Asguard Wheels #3
- Asguard Wheels #4
- Spherical Helical Wheels #1
- Spherical Helical Wheels #2
- Spherical Helical Wheels #3
Mobility Tests

• Comparison of two rover setups:
  ▪ Steering and maneuvers test
  ▪ Slope Driving at 25° inclination
  ▪ Step climbing
    (100-125 mm vs. 310 mm)
  ▪ Crevasse test
    (~200 mm vs. ~300 mm)
  ▪ Static stability up to 40° inclination
• Chosen scout rover setup with helical wheels due to design driver

Locomotion Tests
Coyote II Soil Sensor Integration

Outlook

- Test of autonomous rover-to-rover collaboration
- Soil sensor implementation
- Dual rover team soil examination and traversal tests
- Proof of concept field trials

Final Demonstration Workshop
October 23rd, 2014
Airbus Defence and Space, Stevenage, Great Britain
https://www.faster-fp7-space.eu/
Thank you!

https://www.faster-fp7-space.eu/

Contact

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References


3.4 ‘Moonwalk’ (MD-T-04)

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Abstract

The collaborative EU project MOONWALK aims for the development and test of novel ways in the astronaut - robot interaction. During this project a new rover and a gesture recognition device will be develop at the DFKI. This presentation introduces the projects, its aims and our approach towards them to the scientific staff at the DFKI.
ASTRONAUT-ROBOT COOPERATION

MOONWALK introduction and system presentation

DFKI

Presented by:
Mathias Höckelmann

MOONWALK

Agenda

• Introduction to MOONWALK
  – Simulation campaign setup
• Rover
• Gesture recognition device
Introduction to MOONWALK

Project overview
Test campaigns

• European project
  – Project runtime: 3 years (09/2013 – 08/2016)
  – 7 partners
  – NASA as associated partner

• Targets:
  – Test and develop novel ways of astronaut – robot interaction
  – Build an European network on earth analogue simulations
• Two test campaigns in 2016
  – 1 week of subsea trials at Marseilles (France)
    • Lunar analogue
    • Reduced gravity, crater exploration
  – 2 weeks of trials in Rio Tinto (Spain)
    • Mars analogue
    • Dusty landscape, geological investigations
Simulation setup

Overall setup

DFKI developments

Simulation setup

Overall setup
3.4 ‘Moonwalk’ – Mathias Höckelmann

Simulation setup
Rover configuration
Marseilles / Rio Tinto trials

Rover
Structure and component description
Rover
Requirements

- Surface and underwater operation without major modifications
- Rated depths up to 50m
  - Umbilical for high bandwidth data connection
  - Power supply on board
- Controlled by human through gestures
  - Only minimal autonomy on board (e.g. obstacle avoidance)
Rover
Component placement

1 Sensorhead
2 Battery
3 Computer
4 Axis assembly (4x)
5 Passive joint

Rover
Application setup comparison

- Marseilles
  - underwater

- Rio Tinto
  - surface
Gesture recognition device

Working principle and system layout

Requirements

• Watertight for underwater usage
  – Small to allow placement in-between diver and astronaut suit
• Independent from the rover
  – Fixed to the subjects upper body
• Command gestures to give orders for the rover
  – Autonomous execution of the orders
• IMU placement on upper body of astronaut
• Preprocessing into 'bone model'
• Finger observation to enable more gestures

Thank you for your attention!

Any Questions?
Appendix

For those how are interested

Simulation sites

Marseilles
Map
Simulation sites
Rio Tinto
Map

Simulation sites
Rio Tinto
Landscape
Rover
Center of gravity

Rover
Top view
Minimal setup
Rover
Rear axis max angle
Minimal setup

Rover
Isometric view
Marseilles configuration
Rover
Isometric view
Rio Tinto configuration

Rover
Isometric view
Pool test configuration
3.4 ‘Moonwalk’ — Mathias Höckelmann

Astronaut suit

Ingress

Image credit: COMEX S.A.

Sampling

Image credit: COMEX S.A.
**Astronaut suit**

- Apollo 11 project video
  - [http://www.youtube.com/watch?v=6WlwYHjTyXk](http://www.youtube.com/watch?v=6WlwYHjTyXk)

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**Gesture recognition**

Prototype layout
• Based on ASGUARD V2
• LIMES actuators
• Reused electronics and software

System architecture

• Underwater application
  – Between 10 and 20 meters submerged
  – Umbilical to surface for data connection
• Surface application
  – More than 30 degrees Celsius
  – WiFi mounted on rover
3.5 ‘Nettun’ (MD-P-01)

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Abstract

The main scientific and technical challenge of the NeTTUN project is a robotic maintenance system that enables automation of inspection and exchange of cutter tools for TBM’s (Tunnel Boring Machines). The NeTTUN Consortium, composed of 21 partners all over Europe, has been assembled to address this challenging set of research topics and objectives.
**Present tool change**

Cutting discs (Disc Cutter) and bits, which are crushing or wearing away rock, are placed directly on the tunnelling shield of a tunnel boring machine (TBM). While doing so, the tunnelling shield is rotated and pressed with high pressure against the rock wall. Due to the extreme loading the tools wear out quickly and need to be changed at short intervals. Until today this can be implemented only by human labor. This activity is for the workers extremely stressful and dangerous because the tools are heavy, the work space closely and is frequently applied with pressure (10 bar). The excess pressure is necessary if flooding have to be expected. In order to overcome the pressure conditions, the workers have to go through a decompression chamber.

**Project goal**

In the future, a robot will take over or assist the maintenance task, which should be placed in the field of decorative chamber. To allow the use of robot, first the assembly of the Disc Cutter for the gripper needs to be simplified or rearranged. Loose parts, such as screws may no longer be available.

![Tunnel Boring Machine (TBM)](image)

**Concept / New Disc Cutter Installation**

The new Disc Cutter is locked by sliding blocks. Spindles which are integrated in the tool make the displacement and securing of the pads possible.

The complete assembly (Disc Cutter) weighs about 300kg and is secured by 2 spindles respective 1000Nm torque.

**Concept Gripper with screw mechanism**

The gripper must manipulate the heavy load of roughly 300kg and is able to operate the screw mechanism with 1000Nm. The required screw length is 150mm. For this, the gripper fingers are driven by two hydraulic actuators.

![Disc Cutter Mounted Disc Cutter Dismounted](image)

**Project Partners**

3.6 ‘The FASTER Micro Scout Rover Concept’ (MD-P-02)

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Abstract

The poster introduces the design and evaluation of the micro scout rover Coyote II. First, the general operational approach of the scout rover within the FASTER mission set-up is introduced and second, a technical overview of the system itself is given along with a subset of different locomotion and mobility tests.
The FASTER Micro Scout Rover Concept
Helping exploration rovers travel safer and faster over planetary surfaces

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FASTER Idea and Objectives

Analyzing past and future exploration missions and/or mission scenarios like MER or MSR, a need arises to provide faster and safer traversal of exploration rovers.

The objective of the FASTER project includes the concept development, implementation and demonstration of a system for in-situ evaluation of soil properties:

- to improve the mission safety and
- the effective traverse speeds using
- autonomous collaboration between a primary rover and a small scout rover.

Technical Overview

- Boundary Box: 850 x 580 x 410 mm (l x w x h)
- System mass: 9.2 kg
- Wheel torque: 28 Nm
- Average power: 75 W (approx.)

References:

www.faster-fp7-space.eu
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